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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

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Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	09/921,293	CLARKE ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,23,28,29,34-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39 and 40* is/are allowed.

6)☒ Claim(s) *1-8,10-21,23,28,29,34-38,42 and 43* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan et al, "Phase-Lock Basics" in view of U.S. Patent No. 3,751,979 to Ims.

Egan discloses a first phase-locked loop having a first bandwidth producing a first output signal, and operable to lock into a frequency of an input signal (page 222, 9.2.1), modifying the characteristics of the phase-locked loop to form a second phase-locked loop having a second bandwidth narrower than the first bandwidth, producing a second output signal, and operable to lock into the frequency of the input signal (page 223-224, 9.2.2), and, although not specifically disclosed, it is considered inherent that in phase-locked loops a narrower bandwidth is operable to lock into the frequency of the input signal with greater accuracy and greater immunity to noise than that of a wider bandwidth (see for Example U.S. Patent No. 6,466,069 to Rozenblit et al., column 7, line 54 to column 8, line 1).

Egan also discloses a switch operable to switch the bandwidth of the phase locked loop, and correspondingly switch the output of the phase-locked loop, between the first output signal and the second output signal in response to a change in the frequency and based on a first lock indicator signal wherein the first lock

indicator signal indicates whether the first phase-locked loop is locked into the frequency (page 223-224, 9.2.2).

As noted above, the invention of Egan teaches many of the features of the claimed invention and while the invention of Egan does teach a first phase-locked loop and bandwidth modifier to form a second phase-locked loop, Egan does not specifically include two separate phase-locked loops in a process variable transmitter.

Ims teaches a process variable transmitter (i.e. flow speed measurement system) (column 1, lines 29-30) including two separate phase locked loops (column 16, lines 6-8) and a switch operable to switch the output of the process variable transmitter between a first output of the first phase locked loop and a second output of the second phase locked loop (column 16, lines 26-29 and Figure 8)

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan to include two phase locked loops rather than modifying one phase locked loop, as taught by Ims, because the combination would have provided a faster, simpler, method for switching between two different frequency phase locked loop responses and, as suggested by Ims, provided increased efficiency since the two loops would be continuously driven in desired operation (column 16, lines 54-56).

With respect to claim 2, since the invention of Egan discloses switching the characteristics of the phase-locked loop and the corresponding output signals based upon a lock indicator and the invention of Ims teaches modification of the invention

of Egan to switching between two distinct phase-locked loops, the combination would have included a second lock indicator for generating a second lock indication signal in order to control reverse switching back to the previous loop. Similarly, the combination would have maintained the desired loop in a lock condition while switching to its output to the locked phase-locked loop to obtain the desired bandwidth.

3. Claims 3-5, 8, 13, 21, 34, 35, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan in view of Ims and further in view of U.S. Patent No. 4,463,612 to Thompson.

As noted above, the invention of Egan and Ims teaches many of the features of the claimed invention and while the combination does teach first and second phase-locked loops as well as a flow sensing device, the invention of Egan and Ims do not include the specifics of the phase-locked loops and the flow meter.

Thompson discloses an electronic circuit using digital techniques for vortex shedding flowmeter signal processing comprising a vortex flow sensor (i.e. process variable transmitter) that produces a signal over a line, which varies with the vortex shedding frequency, to a preamplifier, and then over an A.C. coupling to a phase detector (column 2, lines 63-66). Thompson discloses a phase lock loop (column 3, lines 1-4) comprising a phase detector that receives the input signal and produces an output signal to a low-pass loop filter that outputs a filtered signal to a voltage controlled oscillator that feeds-back a locking oscillator signal to the phase detector

(Figure 1). Thompson also discloses including the components of the system on a single low-power digital signal processor chip used for use in a software process (column 3, lines 39-43 and 61-62). Thompson discloses including an amplitude detector (i.e. drop out detector) that senses the amplitude of the input signal and generates a low flow signal when it is below a predetermined level (column 2, lines 13-19).

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan and Ims to include the specifics of the phase-locked loops and flow devices, as taught by Thompson, because Thompson suggests the well-known configurations for a phase-locked loop as required for operation as well as the common construction of a vortex flowmeter that employs phase-locked loops in order to give the invention of Egan and Ims a wider variety of applications in a greater amount of environments.

Further, although not specified, it would have been obvious to one having ordinary skill in the art to allow the user to have more control over the sensing process by specifying that the predetermined low-flow amplitude limit be user-controlled.

4. Claims 29 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan in view of Ims and Thompson and further in view of U.S. Patent No. 5,493,915 to Lew.

As noted above, Egan in combination with Ims and Thompson teaches many of the features of the claimed invention and while the combination teaches an amplitude detector for generating a low flow signal and switching between two phase locked loops, one having a greater immunity to noise, the combination does not specifically teach switching, based upon reception of the low-flow amplitude detector, to the second phase locked loop when a low-flow condition occurs.

Lew et al. teaches a fluid dynamic torsional vortex sensor including a data processor that receives the alternating electrical signal and determines the flow rate with a low flow condition producing a signal with a small amplitude (column 5, lines 9-18).

Since the combination of Egan, Ims, and Thompson teaches switching between a second phase locked loop with a narrow bandwidth, small natural frequency, to provide greater immunity to noise, and a first phase locked loop with a larger bandwidth, large natural frequency, to provide faster locking, it would have been obvious to one having ordinary skill in the art to switch, based upon reception of the low-flow amplitude detector, to the second phase locked loop when a low-flow condition occurs because Lew suggests that the combination would have provided a more accurate result by using the PLL that is less likely to allow noise to interfere with the small amplitude signal.

5. Claims 14-19 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Egan, Ims, and Thompson and further in view of U.S. Patent No. 5,576,497 to Vignos et al.

As noted above, Egan in combination with Ims and Thompson teaches all of the features of the claimed invention except for specifying that the vortex flow sensor sense pressure variations due to vortex shedding of a fluid in a passage, converting the pressure variations to a sinusoidal signal, or pre-filtering the signal processing.

Vignos teaches adaptive filtering for a vortex flowmeter including a well known vortex sensor that produces an analog sinusoidal signal representative of the alternating differential pressure various to calculate fluid flow or velocity (column 2, lines 44-49). Vignos also teaches an initial signal conditioner which filters the signal before subsequent processing occurs (column 2, lines 49-57).

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan, Ims, and Thompson to include specifying that the vortex flow sensor sense pressure variations due to vortex shedding of a fluid in a passage and converting the pressure variations to a sinusoidal signal, as taught by Vignos, because the invention of Egan, Ims, and Thompson teaches the processing method, not the specifics of the sensor itself, and Vignos teaches the well known features and operation of a vortex sensor.

Further, It would have been obvious to one having ordinary skill in the art to modify the invention of Egan, Ims, and Thompson to include pre-filtering the signal before processing, as taught by Vignos, because, as suggested by Vignos, the combination would have provided a method for conditioning the signal to obtain a

desired bandwidth around the vortex frequency and therefore preserved a high signal-to-noise ratio which produces a more accurate flow measurement over a wider variety of flow conditions (column 2, lines 58-67).

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan, Ims, and Thompson and further in view of U.S. Patent No. 6,298,100 to Bouillet.

As noted above, Egan in combination with Ims and Thompson teaches all the features of the claimed invention except for specifying that the phase detectors comprise a heterodyning module and a Hilbert transformer.

Bouillet teaches a phase error estimation method for a demodulator comprising a phase locked loop with a pilot component as a reference and a conventional phase detector for phase acquisition, all part of a phase control loop (column 3, lines 13-17). Bouillet also teaches including a Hilbert filter for receiving the pilot signal, transforming the signal into in-phase and quadrature components, and applying the transformed components to the phase control loop (column 3, lines 31-46). Bouillet also teaches heterodyning the reference pilot with the carrier in the main path of the phase locked loop (column 4, lines 15-30).

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan, Ims, and Thompson to include specifying that the phase detectors comprise a heterodyning module and a Hilbert transformer, as taught by Bouillet, because, as suggested by Bouillet, the combination would have reduced distortion

errors by heterodyning the received spectrum of the phase locked loop down to a baseband (column 4, lines 15-22) as well as produced a phase control signal by correlating received sync values with a Hilbert transform of a reference sync value (column 3, lines 61-65).

7. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan, Ims, and Thompson and further in view of U.S. Patent No. 5,570,300 to Henry et al.

As noted above, Egan in combination with Ims and Thompson teaches all the features of the claimed invention except for specifying that the transmitter include a module for generating uncertainty parameters including a status variable.

Henry teaches self-validating sensors, using software (column 14, lines 40-41), that include a transducer for generating a data signal related to the value of a variable and a transmitter for receiving the data signal and generating output signals, wherein the transmitter generates a first output signal related to the value of the variable and a second output based on a dynamic uncertainty analysis of the first output signal (abstract). Henry also teaches that the uncertainty parameters include a measurement status variable (column 2, lines 17-20) indicating quality (column 7, lines 60-63) based upon the varying frequency of the output signal (column 9, lines 14-27 and column 13, line 61 to column 14, line 22).

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan, Ims, and Thompson to include specifying that the transmitter

include a module for generating uncertainty parameters including a status variable, as taught by Henry, because, as suggested by Henry, the combination would have allowed the user of the sensors to obtain an accuracy measurement of the sensor data since sensors do not perfectly represent the value of a process variable obtained, and often includes effects, such as faults or distortion, resulting from the sensor itself (column 1, lines 20-26).

8. Claims 20 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan, Ims, Thompson and Vignos and further in view of U.S. Patent No. 4,201,084 to Ito et al.

As noted above, Egan in combination with Ims, Thompson and Vignos teaches many of the features of the claimed invention including a prefilter, a low flow detector, and an implicit teaching that low flow conditions produce a small output amplitude in a flow sensor. The combination, however, does not specify that the prefilter is switched on based upon the low flow detection.

Ito teaches a vortex flow meter including a filter switchable between active and inactive states (column 2, lines 10-24) wherein the filter is active when a low flow condition exists (column 7, lines 12-21).

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan, Ims, Thompson and Vignos to include specifying that the prefilter is switched on based upon the low flow detection, as taught by Ito, because, as suggested by Ito, the combination would have provided a method for filtering to

obtain a good signal-to-noise ratio when the amplitude of the flow signal is small thereby enabling better signal detection (column 2, lines 32-46 and column 7, lines 12-21).

9. Claims 23, 28, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egan, Ims, and Thompson and further in view of U.S. Patent No. 5,128,625 to Yatsuzuka et al.

As noted above, Egan in combination with Ims and Thompson teaches all the features of the claimed invention except for providing the output signal of the first PLL to the second PLL as a center frequency of the second PLL.

Yatsuzuka teaches an adaptive phase lock loop system comprising two phase locked loops prepared so that the first PLL caries out on the initial training mode, and the second PLL performs the conventional process so that when the PLLs are initially or periodically initiated, the second PLL is activated with the initial phase and center frequency given by the first PLL after the initial training mode is performed (column 14, lines 14-20).

It would have been obvious to one having ordinary skill in the art to modify the invention of Egan, Ims, and Thompson to provide the output signal of the first PLL to the second PLL as a center frequency of the second PLL, as taught by Yatsuzuka, because, as suggested by Yatsuzuka, the combination would have provided fast accurate results and lock-in by training to obtain optimal values for the

corresponding input signal, thereby insuring that when the second PLL is initiated an optimum center frequency is used (abstract).

Allowable Subject Matter

10. Claim 39 is considered to be allowable over the cited prior art because while the cited prior art does teach a switchable pre-filter the cited prior art does not indicate that this switchable pre-filter replaces the inputs to a PLL when it is on. Therefore, none of the cited prior art teaches or suggests, in combination with the other claimed limitations for a process variable transmitter, a pre-filter wherein, based on a status of the low-flow signal, a fixed center frequency of the second phase-locked loop switchable between an output signal of a first phase-locked loop, and $2\pi f_{ph}$, where f_{ph} is a high cut-off frequency of the pre-filter.

Claim 40 is considered to be allowable over the cited prior art because while the cited prior art does teach a self-validating module that includes status variables of CLEAR, BLURRED, DAZZLED, and BLIND, none of the cited prior art teaches or suggests, in combination with the other claimed limitations for a signal processing apparatus, specifying that the measurement status variable of the self-validating module be CLEAR when both lock indicator signals indicate lock, BLURRED when one of the two lock indicator signals indicates lock and the other of the two lock indicator signals indicates no lock, DAZZLED when both lock indicator signals indicate no lock, and BLIND when both lock indicator signals indicate no lock for at least a predetermined length of time.

11. Claim 9 is objected to as being depended on a rejected claim but would be allowable over the cited prior art if rewritten in independent form including all of the limitations of the base claim and any intervening claims for reasons similar to allowable claim 39.

Response to Arguments

12. Applicant's arguments with respect to claims 1-21, 23, 28, 29, 34-40, 42, and 43 have been considered but are moot in view of the new ground(s) of rejection.

The following arguments, however, are noted.

Applicant first argues that the "disclosure from Ims is not analogous to that in Egan, in which there is only a single input signal. As explained below, the difference in the number of input signals has a variety of important practical implications. Accordingly, one of ordinary skill in the art would not look to Ims to modify Egan."

The Examiner asserts that it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the instant invention, the invention of Ims, and the invention of Egan are all reasonably pertinent to the problem of measuring process variables using different bandwidths of PLL's, and are therefore analogous.

Applicant also argues that "there is no motivation to modify Egan with Ims. Ims mentions that one of the advantages of the FIG. 8 implementation, over the FIG. 5 implementation, is that in FIG. 8 the two PLLS stay in lock whereas in FIG. 5 the single PLL implementation has the delay associated with repeatedly acquiring a new signal and frequency each time the input signal is switched. These conditions, and thus the motivation to use two PLLS, do not exist in Egan" because "there is no indication that modifying Egan with Ims would provide the above advantage of having each PLL stay in lock and avoiding the need to reacquire the signals" and "there is no indication that Egan has the disadvantage of being delayed each time a bandwidth change is made, as described with respect to FIG. 5 of Ims."

The Examiner maintains that the proposed modification and motivation is to modify Egan to include two phase locked loops rather than one phase locked loop that is modified because the combination would have provided a faster, simpler, method for switching between two different frequency phase locked loop responses and, as suggested by Ims, provided increased efficiency since the two loop would be continuously driven in desired operation (column 16, lines 54-56).

Applicant also argues that "[i]n addition to the lack of motivation to combine, neither Egan nor Ims discloses or suggests at least 'a first phase-locked loop . . . operable to lock into a frequency of an input signal' and 'a second phase-locked loop . . . operable to lock into the frequency of the input signal' (claim 1, emphasis

added). As explained above, Egan discloses only a single PLL having different bandwidth characteristics and not two separate PLLS both operable to lock into the frequency of the input signal as recited, and Ims discloses only that two PLLS can operate on different signals and not that both PLLS are 'operable to lock into the frequency of the input signal' as recited."

The Examiner asserts that the limitation for 'a first phase-locked loop . . . operable to lock into a frequency of an input signal' and 'a second phase-locked loop . . . operable to lock into the frequency of the input signal' is not met by the references individually, but is met by the combination of Egan and Ims. The invention of Egan discloses a first phase-locked loop having a first bandwidth producing a first output signal, and operable to lock into a frequency of an input signal (page 222, 9.2.1), modifying the characteristics of the phase-locked loop to form a second phase-locked loop having a second bandwidth narrower than the first bandwidth, producing a second output signal, and operable to lock into the frequency of the input signal (page 223-224, 9.2.2). The invention of Ims then teaches a process variable transmitter (i.e. flow speed measurement system) (column 1, lines 29-30) including two separate phase locked loops (column 16, lines 6-8) and a switch operable to switch the output of the process variable transmitter between a first output of the first phase locked loop and a second output of the second phase locked loop (column 16, lines 26-29 and Figure 8).

Therefore, the combination of one phase locked loop that is modified to have two different bandwidth characteristics that each lock onto the same input signal, as

taught by Egan, with the use of two separate phase locked loops, as taught by Ims, meets the invention as claimed.

Applicant also argues that "neither Egan nor Ims discloses or suggests at least a 'switch operable to switch . . . between the first output signal and the second output signal in response to a change in the frequency (of the input signal), and based on at least one of a first lock indicator signal and a second lock indicator signal' (claim 1). As explained above, Egan does not even have two output signals as recited and, therefore, cannot have a switch switching between such output signals. Further, Egan does not have a switch that switches between any output signals, but only a switch that changes bandwidth characteristics."

The Examiner again asserts that the invention of Egan teaches switching a single phase locked loop between two bandwidth characterizations based on a lock indicator signal and a change in frequency, specifically, "the switch can be opened to restore the desired loop parameters. This process must be controlled from external circuitry, perhaps a timer that is initiated when the loop center frequency is tuned to a new value or the output from a lock indicator" (page 223-224, 9.2.2). This teaching modified by the teaching of Ims to use two separate phase locked loops rather than one single phase locked loop, results in a switch operable to switch between the a first output signal and the second output signal in response to a change in frequency and based on a first lock indicator.

Applicant then states that "[l]ikewise, as explained above Ims does not even have two output signals as recited. Further, as explained below, Ims does not switch in response to a change in the frequency of the input signal, and based on at least one of a first lock indicator signal and a second lock indicator signal as recited. Ims has a switch 208, but switch 208 does not switch in response to a change in frequency (claim 1), but in response to a control signal; no change in frequency is required. Switch 208 also does not switch 'based on . . . a . . . lock indicator signal' (claim 1), but based on the control signal. Indeed, Ims describes switching to a PLL that is out of lock (Fig. 5,. col. 16, lines 45-55), as well as switching to a PLL that is in lock (Fig. 8; col. 16, lines 45-55), revealing that the decision to switch in Ims is not related to whether the PLLS are locked."

First, the Examiner asserts that the invention of Ims does have two output signals as illustrated in Figure 8 ("76"). Further, as noted above, the invention of Ims is not included to teach the switching between the two output signals based on a change in frequency and a lock indicator, since this feature is taught by Egan.

Applicant also indicates that "the Office Action does not address the specific limitations of 'switching . . . from an output signal of the first PLL to an output signal of the second PLL when the lock indicator signal indicates that the second PLL is locked' and 'switching . . . from the output signal of the second PLL to the output signal of the first PLL when the lock indicator signal indicates that the second PLL is

out of lock' (claim 21). One or more similar limitations is also found in claims 34 and 35."

The Examiner asserts that the Office Action stated that "since the invention of Egan discloses switching the characteristics of the phase-locked loop and the corresponding output signals based upon a lock indicator and the invention of Ims teaches modification of the invention of Egan to switching between two distinct phase-locked loops, the combination would have included a second lock indicator for generating a second lock indication signal in order to control reverse switching back to the previous loop".

Applicant further argues that "Yatsuzuka does not disclose or suggest at least "providing the output signal of the first PLL to the second PLL as a center frequency of the second PLL to assist lock-in by the second PLL" (claim 23) and "wherein the second phase-locked loop includes a center frequency input, and the center frequency input is coupled to the first output signal to assist lock-in by the second phase-locked loop" (claim 28). The Office Action points to disclosure in Yatsuzuka at column 14, lines 14-20 in which a training mode is used to determine a center frequency. However, Yatsuzuka clearly states that the purpose of the training mode is to provide an optimum center frequency" (col. 14, line 24). In sharp contrast, the "the first PLL" of claim 23 and "the first phase-locked loop" of claim 28 (which provide the center frequency information in claims 23 and 28) are not recited as providing an optimum center frequency. Indeed, "the first PLL" of claim 23 has a

"fast loop filter having a large natural frequency" (claim 21), and "the first phase-locked loop" of claim 28 has less accuracy and less immunity to noise than the second phase-locked loop (see claim 1). Accordingly, "the first PLL" of claim 23 and "the first phase-locked loop" of claim 28 are presumably non-optimum. In light of this distinction from Yatsuzuka, Yatsuzuka's disclosure does not render it obvious for "the first PLL" of claim 23 and "the first phase-locked loop" of claim 28 to provide center frequency information as recited."

The Examiner asserts that in the invention of Yatsuzuka, the "optimum frequency" is a frequency that is considered optimum because it is the frequency optimum for the particular design that will allow the phase locked loop to become locked-in quickly and stably (column 3, lines 45-49 and column 4, lines 10-27). Therefore, the optimum frequency for the invention of Egan and Ims would still produce the large natural frequency, however, the output of the first PLL to the second PLL would be optimum in that for the particular design of Egan and Ims it would be selected to lock in the second PLL faster and with more stability.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 6,466,069 to Rozenblit et al. teaches a fast settling charge pump biasing circuit that varies the bias when a phase lock loop changes frequency to improve the settling time of the phase locked loop (abstract). Rozenblit specifies

that the phase locked loop includes a phase detector, loop filter, and voltage controlled oscillator, wherein the voltage controlled oscillator feeds back the oscillator signal to the phase detector (Figure 1). Rozenblit also teaches changing the locking frequency of the phase locked loop between a narrow bandwidth, small natural frequency, to provide greater immunity to noise, and a larger bandwidth, large natural frequency, to provide faster locking (column 7, line 54 to column 8, line 1).

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications

from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
February 21, 2005

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800